

Synthesizer Driver Including Basic AO Modulator Alignment

Instruction Manual,

(APPLIES TO SERIAL NUMBERS PRIOR TO sn153400)

iHHS-4-xxx Series

Quad output RF Synthesizer

iHSA-4-xxx Series Quad output RF Synthesizer and Amplifier

Models -

Model	Outputs	Freq'	Freq Range	RF Output
		Doubled	(MHz)	Power
iHHS-4	4	×	20-200	1mW
iHHS-4-e	4	\checkmark	150-350	1mW
iHSA-4	4	×	20-200	1W
iHSA-4-e	4	✓	150-350	0.5W

Options -xxx, combinations possible

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Revision History

Jan 2015:	Added details for the optional independent external control inputs MOD_0,1,2,3,	page 11, 28
June 2015:	Added further detail for power level control	page 7
August 2015:	Reset H/W advised before Write command	
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October 2015: "Link Channels" option included



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1 Overview

The iHHS-4 is a programmable multi-channel RF synthesizer. The iHSA-4 version includes integral hybrid amplifiers. All designs include a quad-channel direct digital synthesizer (DDS), an ARM 32-bit Cortex microcontroller (uC), SDRAM memory and four RF power modules. The uC contains non-volatile FLASH memory for program storage. The uC also provides diagnostic and housekeeping capabilities.

The iHSA-4 is designed to operate with Isomet AO modulators, deflectors, tuneable filters and frequency shifters. The four independent RF outputs each provide >1.2 W power from 20-150MHz and >750mW from 150-200MHz. A block diagram of the driver is shown in Figure 2. External controls are applied through a two high density D-type connectors. External inputs are <u>not</u> necessary to operate the driver.

Example applications:

- a. Highly stable tuneable differential frequency source for heterodyne applications using multiple AO frequency shifters.
- b. High stability tuneable source for Spectroscopy applications using AOTFs
- c. Programmable AO laser scanning applications, requiring non-linear or random frequency sweeps.

The Isomet Synthesizer Driver Tool v2.20 software allows PC control of the driver functions using slider and/or key stroke input. The default resolutions are; frequency 0.001MHz, amplitude 0.01%, and phase 0.01°.

The four operating modes are summarized below.

1.1 Single Tone Mode

The DDS is addressed directly via the Host PC. Each output can be set independently.

Available Functions:

- 10-200MHz Frequency tuning range. (150 350MHz for '-e' extended frequency models)
- 0-360deg Phase shift between outputs
- 0-100% Amplitude control (see section 3)

Typical applications: Frequency shifting, "manual" tuning of AO deflector scan position or AOTF filter pass-band wavelength.

1.2 Sweep or Ramp Mode

Frequency, amplitude <u>or</u> phase can be ramped in value.

For conciseness, only frequency ramps (=chirps) will be described since most AO applications will use this mode. A chirp is generated by rapidly incrementing the frequency. The increment step value and dwell time per increment are user programmable. Each output can be programmed with different ramp parameters.



The frequency ramp is initiated using the GUI or from the external Profile inputs on connector J8

Available Functions:

Independent Up - Down ramp slopes.

Dwell (stop at end value) or no-dwell (return to start value) at end of sweep duration. Set amplitude value for ramp. (remains constant for the ramp duration).

The Chirp mode offers the fastest frequency sweep capability, with a minimum dwell time of 8nsec per frequency increment.

The active data is selected using the GUI or from the external Profile inputs on connector J6.

1.3 Multi-level Mode

The DDS chip contains 16 "profile" registers. These can be programmed to provide up to 16 levels of "modulation". <u>EITHER</u> frequency, amplitude or phase can be "modulated" on one or more RF channels.

Note:

Only one parameter, Frequency, Amplitude or Phase can be changed (= modulated) The switching speed is less than 100nsec. Data in non-volatile

The active data is selected using the GUI or from the external Profile inputs on connector J6

1.4 Image Mode

This is a dynamic mode that allows complex frequency patterns or sequences to be output at rates up to 2Mbytes. F/A/P date defined by the user data is downloaded and stored in 2 x 512Mb SDRAMs, sufficient for 1 million output points.

Features:

User defined pattern generation for AO scanning or filtering applications. Active phase control for precise acoustic beam steering. Data output rate can be defined by internal or external clock/trigger signals

The iHHS/iHSA is controlled via a FPGA with data stored in one of the two internal SDRAMs. These memories are volatile and are programmed from the Host PC at start up. Data is stored as "images". Each image comprises of Frequency, Amplitude, Phase and ancillary 'synchronous' control data. When outputting, each location of the internal memory is addressed in sequence. The RF signal responds to the current data set following a valid clock input. This clock is under user control.

Any frequency profile can be down loaded including uni-directional, bi-directional and random frequency patterns. The key advantage of this mode is that a specific amplitude and phase values can be assigned to each frequency. This permits power programming and beam steering of the RF outputs.

This mode is the most flexible and allows a high data throughput when applying frequency specific amplitude (and phase) control. The minimum dwell time per frequency point is less than 1usec.



The image output trigger and output clock rate can be defined within the Image header data or from the external inputs on connector J6.

1.5 External Hardware

DC Power Supply

Recommended operating voltage is +24Vdc at a current drain of approximately < 2.6A. The external power source should be regulated to \pm 2% and the power supply ripple voltage should be less than 200mV for best results. Higher RF output power is achieved at 28Vdc. A mating power connector is supplied for J8

Air cooling

Free air circulation is required over the driver heatsink. Fan assist is recommended. A small fan is fitted as standard. If the internal driver temperature exceeds 50°C, a warning signal is generated and LED 'F' flashes.

Connector expansion

A connector expansion card is available for the two high density D-types connectors J6 and J7. This interface PCB allows easy connection to the main input and output control signals. A schematic is provided in the Appendices

1.6 PRECAUTIONS

LVTTL digital input levels must not exceed 3.3 volts

Analog input levels must not exceed **5.5 volts** except where shown.

DAMAGE TO THE AMPLIFIER MAY RESULT IF THE TEMPERATURE EXCEEDS 70°C.

SERIOUS DAMAGE TO THE AMPLIFIER MAY ALSO RESULT IF THE MAIN RF OUTPUT(S) IS OPERATED OPEN-CIRCUITED OR SHORT-CIRCUITED.

Before operating the iHSA-4 driver, always terminate the RF output(s) with an AO device or 50Ω load.



2 OPERATION

The manual will first describe basic single tone operation using <u>no</u> external control inputs. Subsequent sections will describe sweep modes, profile select, external control and storage features.

2.1 Install Software.

Run the *setup.exe* from the iHHS Tool directory on the supplied CD or zip file Select and run *Isomet iHHS Tool* from the Start Menu, All Programs. Connect the USB and apply DC power (+18V minimum, +30V maximum)

The title bar will show *Connected* when USB communication is established and give the firmware version number.

This Isomet GUI features tooltip hints. Place the cursor near a wiper or check box to display the corresponding Tooltip.

The iHHS / iHSA will <u>only</u> respond to data changes after the *Write* button at the foot of each page is pressed. Slider controls are one exception. Selected data is auto-written once the respective slider button is released. The *Write* button can also be used to confirm new slider values. It is advisable to press the reset hardware button *Reset H/W* before *Write*. This will place hardware in a known state.

The slider controls snap to the nearest 0.5 unit. Fine control is achieved using the navigation keys.

Keys	FREQ slider	PHASE slider	AMPL slider
+/-	1 MHz	10 °	10%
PgUp / PgDn	0.1 MHz	1 °	1%
↑ / ↓ arrows	0.01 MHz	0.1°	0.1%
\leftarrow / \rightarrow arrows	0.001 MHz	0.01°	0.01%

The opening window will display six menu tabs. Setup, Channel, DAC, ADC, Image and Direct.

The *Direct* tab displays the internal DDS register values and is a low level diagnostic tool.

Most user controls are found under the *Channel* and *DAC* tabs

Before describing the six tabs in detail, we will review the various methods for setting the output RF power.

3 POWER Control, all modes

The output RF amplitude is defined by the combination of 3 controls as described in the following illustration.

The first depends on the operating mode.

The remainder apply across all channels and for all modes.





1 Image Data

- AMPL slider (see: Channel tab). Provides independent 10 bit scaling of the each DDS output. This slider is inactive during frequency and phase RAMP modes.
 - or -
- b. **AMP** file data. Amplitude values defined in the *.ihh *Image* mode files. Provides 10 bit scaling of the DDS output. This method applies to the Image output mode only.

2 DDS (Output Current) Limit

- c. *Current* selection options (re: *Channel* tab). Sets the full scale DDS output current. Four step increments: Eighth(min), Quarter, Half, Full(max). Default=Full
- d. DAC Wiper Control , digitally controlled potentiometers (see: DAC tab,).
 LVL-D sets the DDS chip output current. Default setting=7%

3 Mixer Level

e. Mod_G, an external 0 – 5V input applied to pin 3 of connector J6.

This can be used for high speed dynamic amplitude control and allows RF modulation to be synchronized with connected equipment. Standard = Single common input for all outputs.

Optional = Independent input for each RF output

f. DAC Wiper Control , digitally controlled potentiometers (see: DAC tab,).

LVL-0 sets the pre-amplifier gain.

- or -

LVL-1 sets the pre-amplifier gain.



In most situations, leave the *Current* selection and *LVL-D* settings at the default values.

The user selects the active power control (LVL-0, LVL-1 or External) using the *MdMx* check boxes in the *DAC* tab



RF Modulation/Level Control

Typical full power response at 80MHz for the iHSA-4. RF rise/fall time < 50nsec



4 SETUP tab

The <u>Setup</u> tab allows the user to select the model type, operating mode and set global limits.

Use the *Synthesizer* drop down menu to select the specific iHHS or iHSA model. This will configure the GUI to suit the hardware

Certain models contain frequency doublers to extend the frequency range up to 400MHz. This option is factory fitted. The GUI allows for the multiplication factor provided the correct model is specified.

Isomet Synthesizer Driver Tool v2.46 (Connected to: iHHS)	IO Interface, firmware version Ver 1.02.11)	×
Setup Channel DAC ADC Image Direct		
Selected Target Synthesizer		
Synthesizer: iHSA_4		
Modulation Type (FR1)	(FR2) Enabled Channels	
Mod Level: 2-level Default value: D00000	Default value: 2000	IF Ch3
Ramp Select: RU/RD disabled 💌	Frequency Doubler	Titted Link Channels Enabled
Pin/Channel: 2-level modulation on all channels, no RU/RD	Channel Frequency Con	trol Range
	Min MHz —	60 MHz
Actual value: D00000	Actual value: 2000 Max MHz	100 MHz
Differential Frequency Offset Channel Selection		Sets the upper frequency for each channel frequency tuning w
Offset Channel Range		
Channel 0: No Offset V None V		
Channel 1: No Offset V None V		
Channel 2: No Offret		
Channel 3: No Offset V None V		
Write		Reset H/W

For basic single tone (static frequency) operation, use the default values for the *Modulation Type (FR1)* and *(FR2)* panels as shown above.

Channel Frequency Control Range panel

Set the min-max limits for the frequency control sliders in the Channel Tab.

Enabled Channels □ check boxes

In all cases one or more channels MUST be selected, depending on the active channels required. Ch0 = Channel0 or RF output 1, Ch1 = Channel1 or RF output 2 etc.

Link Channels D check box

When checked, this links all four channels to together. (The *Enabled Channels* check boxes will be greyed out) Channels Ch0, 1,2,3 will output exactly the same Frequency, Amplitude and Phase (F/A/P) values. Ch0 becomes the master. The value(s) set on Ch0 will be applied to the slave channels Ch1,2,and 3. Values on the Slave channels may be subsequently altered.

Link Channels only applies to single tone operation, (see Section 6, Channel Tab).

[Don't forget, press Write to load new values]



5 DAC tab

) Isomet Syn	thesizer Drive	er Tool v2.	23 (Conr	ected to	: iHHS I) Interfa	ace, firmv	vare versi	on Ver 1.	02.11)				×
Setup Char	nnel DAC AI	DC Image	Direct											
P2 Out	er Control		•		_j_			•		•	5.00V	Read DAC		
DAC Wiper Co	ontrol .	1 1	•	•	•	•	•	1 1	•		0.0% 98.4%			
		• •	•		•	•	•	· ·			2.00V 0.0%	Read DAC Store DAC		
PORT C HRP1 HRP2 HRP3 HRP4 INT_TR1	PORT G	Port F - G Bi Ext MdIV ACR ACR	as En 1x0 1x1 4 5 6											
Read	Read Wr	ite										Reset H/1	N.	

The **<u>DAC</u>** tab allows the user to set the output amplitude level and select the control method.

MCU DAC Wiper Control panel:

This is a general purpose DAC output voltage: range 0 - 10V / 30mA (Connector J7, DAC_O) Typical uses: Detector bias, Amplifier bias

DAC Wiper Control panel:

The default settings give maximum output.

- LVL_D limits the DDS chip output current, maximum on RH side (0%) This wiper affects all RF outputs. Always active.
 The % scale is not calibrated to output power. Full range gives approximately 14dB power control, non-linear response. Default value 7%. For most uses, this should not need adjustment.
- LVL_1 sets the amplifier gain, maximum on RH side (100%) This wiper controls all RF output levels. Active only if selected by the MdMx0 / MdMx1 check boxes in Port F panel (see below) The % scale is not calibrated to output power. Full range gives approximately 24dB power control, non-linear response.
- LVL_0 sets the amplifier gain, maximum on RH side (100%) This wiper controls all RF output levels. Active only if selected by the MdMx0 / MdMx1 check boxes in Port F panel (see below) The % scale is not calibrated to output power. Full range gives approximately 24dB power control, non-linear response.



<u>Port F panel</u>:
□ MdMx0,
□ MdMx1 check boxes select the secondary amplitude control / modulation source.

Standard configuration,

A single external modulation input (MOD_G) common to four outputs

Active Control	MdMx0	MdMx1	Comment
None	0	0	OFF (< 37dB)
MOD_G input J6, (0-5V)	0	1	Fast external modulation, common
LVL_0 slider	1	0	
LVL_1 slider	1	1	Default

Optional configuration. Independent external modulation

A separate external modulation input (MOD_0,1,2,3) for each RF output.

Active Control	MdMx0	MdMx1	Comment
MOD_0,1,2,3 input J6, (0-5V)	0	0	Fast external modulation, indep't
None	0	1	OFF (< 37dB)
LVL_0 slider	1	0	
LVL_1 slider	1	1	Default

Typical applications both are checked (=1)

□ G_BIAS : Solid state opto-relay, internal control. This is internally connected to the power amplifier stage of the iHSA-4. <u>Un</u>checked = Logic low = RF outputs enabled = Left orange LED "C"



Note: a fault condition e.g. over temperature, will override this control and disable outputs

□ Ext-EN : Solid state opto-relay, external control. Floating contacts, 8 ohms on-resistance, 150mA, 100V max. Available for external equipment control (Connector J7, EQ_En) Unchecked EXT_EN = closed contacts = Left red LED "D"

□ ACR4...7 : Reserved for future use Box checked = Logic high (3v3)

Port G panel: ☐ **Bit3..0** = Read only. ☐ **Bit7..4** = General purpose digital I/O. Reserved for future use Box checked = High (3v3)

Port C panel: □ HRP1..4 = Read only signal monitor. Applies to RFA1160-4 Power amplifier only □ INT_TRI = Reserved for future use

Box checked = High (3v3)



6 CHANNEL tab

The *Channel* tab, is the main frequency control window. .

The user may enter values for Single Tone (static frequency) operation, Multi-level modulation and RAMP programming

Basic features:

User defined Frequency slider range, limits set under **Setup** tab. 0-360deg Phase shift between outputs 0-100% Amplitude control

Configurations can be saved to PC disk

Frequency tuning response is limited by the speed of the USB II communication

Single Tone mode

Setup Channel DAC IDDE Image Direct Channel 0 Channel 1 Channel 2 Channel 3 FREQ PHASE AMPL	
Channel 0 Channel 1 Channel 2 Channel 3 FREQ PHASE AMPL 200 360 100	
FREQ PHASE AMPL 200 360 100	
200 360 100	
80.000 0.00 50.00 (%) (MH2) (%) (%)	
Channel Function Reg Config	
Default value: 000000 AFP Select: Disabled 💌 Sweep Options: Step 💌	
Actual value: 000300 Current: Full scale V Sweep Type: No dwell V	el
	•
Write Reset H/W File Load File	we

Only the channels enabled under the **Setup** tab will be displayed Use the sliders to adjust and set the output frequency, phase and amplitude scaling.

Each channel is set independently. Select the appropriate **Channel** slider group tab. In the screen shot above, only two channels have been selected

Config panel: The profile inputs [P0...3] are multi-purpose. Their function depends on the operating mode. Not used for the basic single tone operation.

[Don't forget, press *Write* to load new values] [Also check *DAC* tab, Port F, **G_BIAS** = <u>un</u>checked to enable RF output for iHSA-4]

This completes the basic driver configuration. Refer to Installation and AO Alignment section.



6.1 Ramp or Sweep mode

Typical mode for AO Scanning applications, non-beam steered AO deflectors

a. To enable frequency, phase or amplitude sweep modes, the *Mod Level* under the *Setup* tab must be set to *2-level*

Store Channel Synthesizer Driver Tool V 2.32 (connected tox HHS 10) Interface, formware version Ver J.02.11) X Selected Target Synthesizer Selected Target Synthesizer Synthesizer Coverd I Default value: D00000 Proj Channel: Perform Type (FR1) Modulation Type (FR1) Perform Type (FR1) Projection Type (FR1) Proj Channel: 2000 Program Type (Tot Tot Tot Tot Tot Tot Tot Tot Tot Tot				
Stetus Channel DAC Image Direct Selectod Target Syntheszer	Isomet Synthesizer Driver Tool v2.23 (Connected to: iHHS)	10 Interface, firmware	version Ver 1.02.11)	<u>×</u>
Selected Target Synthesizer Synthesizer Synthesizer Synthesizer Modulation Type (FR1) Pin/Channels Pin/Channels 2/evel modulation on all channels, no BU/RD Actual value: D000000 Actual value: D000000 Mattin Value: D000000 Actual value: D000000	Setup Channel DAC ADC Image Direct			
Synthesize: Course I Modulation Type (FR1) Mod Lee: 2-lord I Ph(/Chandle 2-lerd modulation on all chandle, no RU/RD I Actual value: 2000 Actual value: 2000 Write Write Mod Lee 2-lord I Mod Lee 2-lord	Selected Target Synthesizer			
Moduletion Type (FR) Default value: Down Mod Level: 2-fevel I Default value: Down Pin/Channels: 2-fevel modulation on all channels, no RU/RD I Actual value: 2000 Actual value: D000000 Actual value: 2000	Synthesizer: Generic -			
Mod Level: 2-level Default value: D000000 Ranp Select; RulPD disabled Default value: 2000 Projector; Default value: 2000 Frequency Doubler Actual value: D000000 Actual value: 2000 Write Mod Level: 2000 In Mit; Write Mod Level: 2000 Reset:				
Mod Levis 2-loved T Defruit Value: D000000 Ramp Select1 RU/RD diabled T Pin(Channel: 2-loved modulation on all channels, no RU/RD T Actual value: D000000	Modulation Type (FR1)	(FR2)	Enabled Channels	
Party Select, RU/RD disabled Image: Channels, no RU/RD Phi/Channel: 2-level modulation on all channels, no RU/RD Actual value: D000000 Actual value: D000000 Max Mitz 2000 MHz Virite Reset: H/W	Mod Level: 2-level Default value: D00000	Default value: 2000	I Ch0 I Ch1 I Ch2 I Ch3	
Write Image: Channels, in the RU/RD * Actual value: D000000	Ramp Select: PU/PD disabled		Frequency Doubler	
Pin/Chennel: 2-level modulation on all channels, no SU/KD * Actual value: D000000 Actual value: 2000 Hax HHz 2000 MHz			Changed Stream Control Dog	
Actual value: D000000 Actual value: 2000 Max HHz 200 MHz Write Write Reset: H/W Reset: H/W Reset: H/W	Pin/Channel: 2-level modulation on all channels, no RU/RD		Min MHz	10 MHz
Actual value: [2000] Max MHz 200 MHz				10 1012
	Actual value: D00000	Actual value: 2000	Max MHz	200 MHz
	·			
Write Reset H/W				
Write Reset H/W				1
	Write			Reset H/W

b. The sweep modes are selected under the *Channel* tab.

Some	Synthes	izer Dr	iver Tool v2.2	3 (Connecte	d to: iHHS IO Interface, firmware version Ver 1.02.11)		
Setup	Channel	DAC	ADC Image	Direct			
Channel	0 Cha	nnel 1	Channel 2	Channel 3			
50 200 	PHASE 360 0 0 0,00 (°)	AMPL 100 - - - - - - - - - - - - - - - - - -	E0 200 - - - - - - - - - - - - - - - - -	FSRR:	Ramp up points: 5000 Delta T: 600000 Period: 0.3200000 Actual FDW Value: 78.0000742/day Ramp down points: 100 Delta T: 1200000 Period: 0.3200000 Actual FDW Value: 1990.0000712/day		
Default 1 Actual vi	value: 00 alue: 8	00000	A	FP Select: Current:	Frequency Sweep Options: Ramp Full scale Sweep Type: No dwell		
			Write			Reset H/W	File Load File Save

In the screen shot above, a frequency ramp on Ch1 is selected. Start sweep (S0) 54MHz, End sweep (E0) 93MHz. Rising slope 300us total duration, 500 points, falling slope 120us and 100 points Full scale amplitude selected. Ramp mode, No dwell. Explanation below

Channel Function Register Panel

AFP Select pull down menu selects the parameter to be swept; Frequency, Phase or Amplitude. The fundamental slider is assigned the start value and an additional slider is displayed to set the end value.

Sweep Options pull down menu selects the sweep mode;

- Step is an instantaneous shift between two selected points.
- Ramp is a series of incremental steps between the start (S0) and end (E0) values.



Sweep Type pull down menu selects the sweep characteristic for the RAMP mode only ;

- **No Dwell**: output returns to the start value immediately the end value is reached.
- Dwell: output ramps up on the +ve edge and down on the -ve edge of the control P0 (P1,2,3)

[Don't forget, press Write to load new values]

c. Linear Sweep Settings panel

If *Ramp* is selected, an addition panel is displayed allowing the user to program the rising and falling ramp characteristics. Uni- or bi-directional sweeps may be applied to either Frequency or Phase. (A limitation in the DDS chip prevents an amplitude ramp in this mode).



The RSRR slider defines the duration of the rising slope increment.

The value is displayed in the Delta T window

The number of rising ramp points are entered into the *Ramp up points* window. The total rising ramp time is displayed in the *Period* window.

FSRR slider and *Ramp down points* similarly define the falling slope. The falling slope only applies if *Dwell* is selected in the *Sweep Type* pull down menu.

For correct initialization, please ensure non-zero values in BOTH Delta T windows

(e.g. move the RSRR or FSRR slider at least 1 tick)



Both plots show a ramp on Ch1 ramp (output J2), controlled using input P1



The sweep is initiated by toggling the profile input (P0..3) associated with the selected channel. All the Profiles Inputs are displayed in the **Config** panel under the **Channel** tab

> P0 = Channel 0 sweep control = RF output J1 P1 = Channel 1 sweep control = RF output J2 P2 = Channel 2 sweep control = RF output J3 P3 = Channel 3 sweep control = RF output J4

Check box *Ena* enables Ramp control using the P0..3 control inputs.

Check box *Psel* selects the source of the P0..3 sweep control inputs.

☑ Psel checked (high), selects external P0..3 inputs on the connector J6

□ *Psel* unchecked (low), selects USB/PC control of *P1* and *P2* check boxes, shown in the *Config* panels of this GUI.

[Don't forget, press Write to load new values]

d. <u>Step mode</u> is a two level sweep. It is essentially the same as 2-level modulation

Somet	Synthes	izer Driv	rer Tool v2	3 (Connected to: iHHS IO Interface, firmware version Ver 1.02.11)	×
Setup	Channel	DAC	ADC Imag	Direct	
Channel	0 Cha	nnel 1	Channel 2	Channel 3	
FREQ	PHASE	AMPL	CW1		
200	360	100	200		
1	1	-	1		
-	1				
	1.1	•			
	1.1	1			
1		T	문		
-					
-		-	•		
- i					
	1		•		
1	1.1	-	1		
10	<u>,</u>	<u> </u>	10		
54.000 (MHz)	0.00 (°)	50.00 (%)	93.000 (MHz)		
Channel	Function F	Rea			Config
Default v	value: 0	00000		FP Select: Frequency V Sweep Options: Step V	
Actual va	alue: 8	08100		Current: Half scale Sweep Type: No dwell	□ P1 □ P <u>5</u> el □ P2 □ Ena
_		W	/rite		Reset H/W File Load File Save

Step mode may be applied to the Frequency, Amplitude or Phase. In the example screen shot above, frequency will switch between 54 and 93MHz Also *Half scale* amplitude selected. *Dwell/No dwell* has no function.





6.2 *Multi-level modulation*

Typical mode for AOTF or multi-spot deflector applications.

The DDS chip contains 16 "profile" registers. These can be programmed to provide up to 16 levels of "modulation". <u>EITHER</u> frequency, amplitude or phase can be "modulated", on one or more active RF channels.

The maximum number of levels per output is given by the relatonship: $2^{(Active channels)} x modulation levels = 16$

a. Under **Setup** tab, refer to the **Modulation Type (FR1)** panel For this explanation we will configure for 8-level frequency control on Channel 0(output J1)

Mod Level pull down menu, select 8-level

Ramp Select pull down menu, leave at *RU/RD disabled*. (If enabled, introduces automatic amplitude ramping of the DDS output)

Pin/Channel pull down menu, selects the active channels and control pins Example select *8-level modulation on Ch0*

Isomet Synthesizer Driver Tool v2.23 (Connected to: iHHS IO Interface, firmware	version Ver 1.02.11)
Setup Channel DAC ADC Image Direct	
Selected Target Synthesizer	
Mod Level: Hevel = Merel = Default value: [F82] Mod Level: Hevel = Merel = Default value: D000000 Bang Select: Hevel = Merel = Default value: 2000 Hord Level: Hevel = Merel = Default value: 2000 PhylChannel: Level = Merel	Enabled Channels □ C do C fot C do 3 Frequency Doubler □ Progenery Doubler □ Channel Requercy Control Range
Actual value: 000200 Actual value: 2000	Min MHz 200Hz Max MHz 200 MHz
Write	Reset H/W

[Don't forget, press Write to load new values]

b. Select the Channel tab

For Channel 1, set AFB Select to Frequency

An additional 7 wipers will be displayed, allowing a total of 8 frequencies to be set. Adjust sliders to desired values.



Setup	Channel	DAC	DC Ima	ge Direc						
Channe	10									
FREQ	PHASE	AMPL	CW1	CW2	CW3	CW4	CW5	CW6	CW7	
200	360	100	200	200	200	200	200	200	200	
		Γ				-	-			
	:	-					-			
	1				· ·		-		•	
A	1								•	
		-								
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	1	-	-	1.1	- ÷	-	-	•	•	
11	1			T.						
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	1.1	-	-	-		-	-		•	
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t I I										
11	:						-			
	<u>,</u>	- I	20	20	20	20	20	20	20	
33.500 (MHz)	0.00 (°)	100.00 (%)	128.000 (MHz)	103.500 (MHz)	108.500 (MHz)	140.500 (MHz)	122.500 (MHz)	82.000 (MHz)	141.000 (MHz)	
Channel	Function	Reg			_					onfig —
Default	ralue: 0	00000		AFP Selec	t: Fr	equency 💌	Sweep	Options:	Step 💌	P0 □
Actual vi	lue: 8	08300		Curren	t: F	ull scale 💌	Swee	p Type:	No dwell 💌	P1 🔽
										PZ I

[Don't forget, press Write to load new values]

c. Output control

The driver outputs respond to the set modulation levels by means of the 4 profiles inputs P0,1,2,3

P0 corresponds to Ch0 (iHSA output J1) P1 corresponds to Ch1 (iHSA output J2) P2 corresponds to Ch2 (iHSA output J3) P3 corresponds to Ch3 (iHSA output J4)

Modulation Level	Profile Control	Active Channels
	P0 = MSB	
16 Lovol	P1	000
10-Level	P2	One
	P3 = LSB	-
	P0 = MSB	
8 L ovol	P1	000
0-Level	P2 = LSB	One
	P3 = X	9
4 aval	P0 = MSB	Two
4-Level	P1 = LSB	TWO
4	P2 = MSB	Two
4-Level	P3 = LSB	IWO

Check box *Ena* enables control using the P0..3 control inputs.

Check box *Psel* selects the source of the P0..3 sweep control inputs.

☑ Psel checked (high), selects external P0..3 inputs on the connector J6

□ *Psel* unchecked (low), selects USB/PC control of *P0,1,2* and *P3* check boxes, shown in the *Config* panels of this GUI.

[Don't forget, press Write to load new values]



6.3 File Save and Load

The *File Save* and *File Load* features available at the foot of the *Channel* tab allow the operating settings for the iHSA to be saved on and recalled from the host PC.

This includes all parameters for the Ramp and Miult-level modulation modes.

7 ADC tab

The ADC tab provides diagnostic feedback

) Isomet Sy	nthesizer Driver Tool v2.23 (Connected to: iHHS IO Interface, firmware version Ver 1.02.11	L)			×
Setup Cł	nannel DAC ADC Image Direct				
ADC Input	s				
Fwd 1		0.00%	Scaled		
Fwd 2		0.00%	C Hex		
Fwd 3		0.05%			
Fwd 4		0.07%	Read Analogs		
Ref 1		0.00%			
Ref 2		0.00%			
Ref 3		0.00%			
Ref 4		0.00%			
Idc 1	<u></u>	0.00A			
Idc 2	<u></u>	0.00A			
Idc 3		0.00A			
Idc 4		0.00A			
Ext-T		0.0°			
Int-T		0.3°			
Vdc		24.85V			
An-IN		0.04V			
	Write			Reset H/W	
			_	toot in the	

- An-In: (uses AIN15) Measures the voltage applied to connector J7, AIN15 General purpose ADC voltage input for external use. Maximum applied voltage +10V, minimum 0V, current 6mA.
- VDC: (uses AIN14) DC voltage applied to iHSA-4. Accuracy +/-5%
- *Ext_T*: (Option). Displays the temperature of external equipment fitted with an AD590 sensor circuit.
- *Int_T*: Displays the temperature of the iHSA-4 heat sink
- *Fwd 1..4* : (Indicates forward RF power. Option for use with RFA1160-4 only).
- Ref 1..4: (Indicates reflected RF power. Option for use with RFA1160-4 only).
- Idc 1..4: (Indicates power amp supply current. Option for use with RFA1160-4 only).

[Don't forget, press *Read Analogs* to update values]



8 IMAGE tab

The *Image* tab allows the user to control and program the iHSA output(s) using externally generated data files. The format must adhere to the *Image File Format* specification (see Section 17.2) and Isomet Image Generator Software is available to simplify Image file generation.

To view and edit Image these files, we recommend downloading hex editor software such as Hex Editor Neo by HDD Software Ltd.

Data can be loaded into one or both SDRAM memories and may be loaded into Bank1 whilst Bank0 data is outputting and visa-versa. Thus the user can flip-flop the load and play actions between memory banks.

Sequence:

Select Bank 0 Image File or Bank 1 Image File panel Browse for the location of the file Press Send Press Run

) Isomet Synthesizer	r Driver Tool v2.23 (C	onnected to: iHHS 10 Interface, firmware	version Ver 1.02.11)	×
Setup Channel DA	AC ADC Image Di	ect		
Bank 0 Image File				
Image file:	C:\Users\Mike\E	ropbox\HigherSynth\Excel-BS-AODs\	LS110\iHH files\Evr_12imgRp	t_Dots_Sq_clk11_P2_Sqrs.ihh Browse
				Send Run Bank 0
				Outputting bank 0
Bank 1 Image File				
Image file:	C:\Users\Mi	ke\Dropbox\HigherSynth\Excel-BS-AC	DDs\LS110\iHH files\Evr_12in	gRpt_81pt_clk02_P2_Sqrs.ihh Browse
				Send Run Bank 1
				Outputting bank 1
Image Status				
FPGA version:	1_5_159 Input	ank: 0 Output bank: 1	Image output status: running	Stop Output
	SOI cou	nt: 16421	Image in progress: 4 (")	Refresh Status
	DA state	e: 1	Tacho count: 129	
	Status u	pdates: 133	Repeats: 15	
	Write			Reset H/W

RF power limits are set under the **DAC** tab.

Image status panel provides diagnostics and progress of the outputting file.

A file may contain more than one Image and each Image may be repeated. Tacho indicates the current frequency point being output.

The iHSS/iHSA can be programmed to generate additional digital and analog control signals on connector J6. These are synchronous to the RF output generation and thus enables the iHHS/iHSA to be used as master controller in complex laser systems.

The image file header data defines the output clock and trigger signal parameters. If external signals are selected, these are connected to J6



9 DIRECT tab

The *Direct* tab provides readback of the internal registers in the DDS chip This is for diagnostic purposes.

Values can also be input directly and edited in this mode. Use this method with Caution.

Somet S	Isomet Synthesizer Driver Tool v2.23 (Connected to: iHHS IO Interface, firmware version Ver 1.02.11)								
Setup C	hannel DAC AD	Channel 2 Channel 2	1						
Channer	Channel 1		1						
CFR	808300	CW1	4189374B	CW8	0A3D70A3				
CFTW0	2AC08312	CW2	0A3D70A3	CW9	0A3D70A3				
CPOW0	0000	CW3	0A3D70A3	CW10	0A3D70A3				
ACR	0013FF	CW4	0A3D70A3	CW11	0A3D70A3				
LSRR	0000	CW5	0A3D70A3	CW12	0A3D70A3				
RDW	00000000	CW6	0A3D70A3	CW13	0A3D70A3				
FDW	00000000	CW7	0A3D70A3	CW14	0A3D70A3				
				CW15	0A3D70A3				
	Contro	Registers							
	CSR	04 FR1 D000	00 FR2 2	000	Read	Erase Flash			
	Wri	te				Reset H/W			



10 LED Indicator and Monitor outputs

The two front panel tri-colour LED sets indicate the operating state.



Top left BLUE - A: Normal condition is ON

LED will illuminate BLUE when DC power is applied.

Middle left GREEN - B: Normal condition is Beating ON-OFF

LED will every illuminate GREEN every 3 seconds when initialization is completed

Middle left ORANGE – C: Normal condition is ON

LED will illuminate ORANGE when G_BIAS is active and RF power amplifiers are enabled. LED will not light if :

- external interlocks are not connected
- driver heatsink temperature exceeds 50degC
- G_BIAS not enabled (un-checked) in software

Bottom left RED - D:

LED will illuminate RED when Ext_En is active and external equipment is enabled. (if connected)

Top right BLUE - E: Normal condition is OFF

LED will illuminate BLUE when there is a fault condition. Fault conditions:

- DC power is below 15Vdc or above 28Vdc
- Driver over temperature.

Middle right GREEN – F: Normal condition is ON

LED will illuminate YELLOW when the DC supply voltage is within limits Limits: 30V > v > 15V

<u>Middle right ORANGE – G:</u> Reserved for future use

Bottom right RED – H: Normal condition is OFF, not blinking

LED will blink RED when driver temperature is outside recommended limits Limits: $50^{\circ}C > T > 7^{\circ}C$.



11 Resetting

To correct a fault condition, it will be necessary to reset the driver.

- USB communication is operating:
- a. Using the GUI, press the **Reset H/W** button on lower right of screen. - or -
- b. RESET the driver by momentary connecting pin 12 to pin 25 on J7
 - USB./ Isomet GUI not operating:
- c. Turn the DC power OFF and ON - or -
- d. RESET the driver by momentary connecting pin 12 to pin 25 on J7

12 Installation and AO alignment

The procedure below applies to all type of AO devices operating at a fixed centre frequency. This method may also be used for the initial alignment of swept frequency devices such as AO deflectors and AOTF's. See Figure 3, however the initial procedure uses the Isomet GUI only and requires no external control inputs.

Adjustment of the RF output power is best done with iHSA driver connected to the acousto-optic device. When shipped, the iHSA driver output power is set to give 250mW maximum per output at 80MHz.

The optimum RF power level required for the modulator to produce maximum first order intensity will be differ depending in the laser wavelength. Applying RF power in excess of this optimum level will cause a decrease in first order intensity (a false indication of insufficient RF power) and makes accurate Bragg alignment difficult. It is therefore recommended that initial alignment be performed at a low RF power level.

- a. With the DC power supply off, connect the DC power to input J8.
- b. Connect the SMA connectors J1, J2, J3 and J4 to the acousto-optic RF inputs or to 50Ω RF load(s).
- c. Connect the Interlock connector J5 (mini 4-pin snap type). Connection is made to the <u>Interlock</u> of the acousto-optic device or to a mating plug with shorting link. (supplied, see page 30).
- d. Apply the DC supply voltage.

At this stage, ensure there are no connections to the high density connectors J6 and J7. The initial alignment should be made at the AO centre frequency at less than half RF power. Referring to the single tone basic setup described above;



e. Tune the iHSA-4 frequency to match the AO centre frequency using the *FREQ* slider Adjust the RF power by setting the *AMPL* slider to 30%

Check in **DAC** tab:

LVL_D = 7% LVL_1 = 100% (Port F) MdMx0 is ☑ MdMx1 is ☑ G_BIAS is □

[Press Read buttons to update]

f. Input the laser beam toward the centre of either aperture of the AOM. Ensure the polarization is correct for the AO crystal and the beam height does not exceed the active aperture height of the AOM. Start with the laser beam normal to the input optical face of the AOM.

Observe the diffracted first-order output from the acousto-optic modulator and the undeflected zeroth order beam. Adjust the input angle (rotate the modulator) very slightly to maximise the first order beam intensity.

g. After the input angle has been optimized, slowly increase the RF power by increasing the AMPL slider until maximum intensity is obtained in the first order.

The RF power may also be adjusted using the digital pot settings as described in the **DAC** tab section

12.1 AO Scanning applications, non-Image mode

Follow the above procedure to set the AO device Bragg angle and RF power. Use the RAMP or Multi-level modes as described above setting the highest and lowest frequencies within the AO device bandwidth limits.



12.2 AO scanning applications, Image mode

Follow the above procedure to set the AO device Bragg angle and RF power. Use the Image modes to input the appropriate image file If an AO deflector is supplied with the iHSA-4, example Image files will usually be provided.

Refer to Application Note: Using the Image File Generator.

Example: Beam steered AO deflector at 830nm

Image Data file: Evr1_LS_128pt_P2_clk08_fc161_A130-600-2-2.ihh Description: Repeating line scan of 128 frequency points Internal output clock set with 8usec period Frequency sweep centred at 160MHz Amplitude weighted to compensate for PA frequency response

Resultant RF power sweep



<u>Set-up</u> (Ext Clock not required for the test file above)

(cont'd)





Measured optical power of scanned first order beam

Continuous uni-directional scans



Vertical Scale: First Order Diffraction Efficiency (DE), 0% to 100% as shown

Horizontal Scale: Drive Frequency, 120 MHz to 200 MHz, as marked



13 AO device maintenance

Cleaning

It is of utmost importance that the optical apertures of the AO device are kept clean and free of contamination. When the device is not in use, the apertures may be protected by a covering of masking tape. When in use, frequently clean the apertures with a pressurized jet of filtered, dry air.

Over time it may be necessary to wipe the A/R coated optical surfaces of atmospherically deposited films. Although the coatings are hard and durable, care must be taken to avoid gouging of the surface and leaving residues. It is suggested that the coatings be wiped with a soft ball of brushed (short fibres removed) cotton, slightly moistened with clean alcohol. Before the alcohol has had time to dry on the surface, wipe again with dry cotton in a smooth, continuous stroke. Examine the surface for residue and, if necessary, repeat the cleaning.

Troubleshooting

No troubleshooting procedures are proposed other than a check of alignment and operating procedure. If difficulties arise, take note of the symptoms and contact the manufacturer.

Repairs

In the event of deflector malfunction, discontinue operation and immediately contact Isomet or local representative. Due to the high sensitive of tuning procedures and the possible damage which may result, no user repairs are allowed. Evidence that an attempt has been made to open the optical head will void the manufacturer's warranty.



14 Technical Specifications,

Maximum Frequency Bandwidth	n (full range): Option -e:	10 – 200 MHz 150 – 350 MHz
Outputs:		Quad independent outputs, phase continuous
Maximum Output Power per out	tput: iHSA-4 iHHS-4	31dBm typical. (>1.2W) 0dBm typical. (>1mW)
Peak power adjustment range: Output power flatness: Harmonics:		 >20dB via digital potentiometer < +/- 1dB per octave, with no amplitude programming > 25dBc
Frequency resolution (full range Frequency stability	e):	32 bit +/- 50ppm Internal reference clock, common to all outputs
Frequency settling time: Max' frequency sweep rate (Rat	mp mode):	< 100nsec 5 MHz/usec, typical
Max' data output rate (Image m	ode):	Single active output: 2.0MHz Dual active outputs: 1.0MHz Quad active output: 0.5MHz
Phase resolution: Phase control:		14 bit +/- 180deg differential between outputs
Amplitude resolution: Amplitude modulation, external * Available configuratio	input(s) *: ons	10 bit 0 – 5V (zero to max) One input all channels (standard), Override, Disable One input per channel (option),
RF On:Off modulation contrast	ratio:	>37dB
DC Supply:		+24V nominal @ 3A iHSA-4 ; 0.7A iHHS-4 (Input voltage range +18V to +30V)
Communications:		USB II, 480Mbps.
Logic / Control Inputs: Analog Inputs:		+3V3 logic compatible, +5V tolerant 0V minimum, +5V maximum, except where specified.
Memory capacity:		1M frequency data points per bank (4 active channels per point)
Mechanical package:		Aluminium shielded case. See Figure 1



15 Connection Summary

Туре
Digital
Analog
Isolated Contact, rated 100V, 150mA max
Input
Output
Bidirectional
Do Not Connect
Digital Ground
Analog Ground
Not connected

J8 DC VOLTAGE INPUT J8-Cable TA3F

J8 DC pov	ver	3 way XLR TINI Q-G		+Vdc (24V)
<u>Pin</u>		Description	<u>Type</u>	0Vdc
3		-	A 1	Female Cord Plug
2	Vdc	12-28Vdc, 2A	A_In A_In	Rear side solder receptacle view

J6 Control 1

40 way Amplimite High Density IDC D-type

<u>Main</u>	(Options)	Main Description	<u>Type</u>	<u>Pin</u>	
EXT_TRG		External Trigger	D_In	40	DGnd
EXT_CLK		External Clock	D_In	39	DGnd
SDOR0		Sync Reg bit0	D_Out	38	DGnd
SDOR1		Sync Reg bit1	D_Out	37	DGnd
SDOR2		Sync Reg bit2	D_Out	36	DGnd
SDOR3		Sync Reg bit3	D_Out	35	DGnd
SDOR4		Sync Reg bit4	D_Out	34	DGnd
SDOR5		Sync Reg bit5	D_Out	33	DGnd
SDOR6		Sync Reg bit6	D_Out	32	DGnd
SDOR7		Sync Reg bit7	D_Out	31	DGnd
P0	(SDOR8)	Profile 0	D_In	30	DGnd
P1	(SDOR9)	Profile 1	D_In	29	DGnd
P2	(SDOR10)	Profile 2	D_In	28	DGnd
P3	(SDOR11)	Profile 3	D_In	27	DGnd
X_BANK		Ext Memory bank Select	D_In	26	DGnd
OHL		NC	D_In	25	DGnd
SDAC_0	* MOD_0	Sync DAC Analog Output	A_Out /(* A_In)	24	AGnd
* MOD_G	* MOD_1	Analog Modulation In, all channels	A_In	23	AGnd
nc	* MOD_2	NC	A_In	22	AGnd
nc	* MOD_3	NC	A_In	21	AGnd
	Main EXT_TRG EXT_CLK SDOR0 SDOR1 SDOR2 SDOR3 SDOR4 SDOR5 SDOR6 SDOR6 SDOR7 P0 P1 P2 P3 X_BANK OHL SDAC_0 * MOD_G nc nc	Main (Options) EXT_TRG EXT_CLK SDOR0 SDOR1 SDOR1 SDOR2 SDOR3 SDOR3 SDOR4 SDOR5 SDOR5 SDOR6 SDOR7 P0 P1 (SDOR10) P3 (SDOR10) P3 (SDOR10) SDAC_0 * MOD_0 * MOD_G * MOD_1 nc * MOD_3	Main(Options)Main DescriptionEXT_TRGExternal TriggerEXT_CLKExternal ClockSDOR0Sync Reg bit0SDOR1Sync Reg bit1SDOR2Sync Reg bit2SDOR3Sync Reg bit3SDOR4Sync Reg bit5SDOR6Sync Reg bit6SDOR7Sync Reg bit7P0(SDOR8)P1(SDOR9)P1(SDOR9)P2(SDOR10)P3(SDOR10)P3(SDOR10)P4NCSDAC_0* MOD_0SDAC_0* MOD_1Analog Modulation In, all channelsnc* MOD_3NC	Main(Options)Main DescriptionTypeEXT_TRGExternal TriggerD_lnEXT_CLKExternal ClockD_lnSDOR0Sync Reg bit0D_OutSDOR1Sync Reg bit1D_OutSDOR2Sync Reg bit2D_OutSDOR3Sync Reg bit3D_OutSDOR4Sync Reg bit4D_OutSDOR5Sync Reg bit5D_OutSDOR6Sync Reg bit6D_OutSDOR7Sync Reg bit7D_OutSDOR7Sync Reg bit7D_OutP0(SDOR8)Profile 0D_InP1(SDOR9)Profile 1D_InP2(SDOR10)Profile 2D_InP3(SDOR11)Profile 3D_InY_BANKExt Memory bank SelectD_InOHLNCD_InSDAC_0*MOD_0Sync DAC Analog OutputA_Out /(* A_In)*MOD_G*MOD_1Analog Modulation In, all channelsA_Innc*MOD_3NCA_In	Main(Options)Main DescriptionTypePinEXT_TRGExternal TriggerD_ln40EXT_CLKExternal ClockD_ln39SDOR0Sync Reg bit0D_Out38SDOR1Sync Reg bit1D_Out37SDOR2Sync Reg bit2D_Out36SDOR3Sync Reg bit3D_Out35SDOR4Sync Reg bit4D_Out31SDOR5Sync Reg bit5D_Out31SDOR6Sync Reg bit6D_Out31SDOR7Sync Reg bit7D_Out31P0(SDOR8)Profile 0D_In30P1(SDOR9)Profile 1D_In29P2(SDOR10)Profile 3D_In29P3(SDOR11)Profile 3D_In21SDAC_0* MOD_0Sync DAC Analog OutputA_Out /* A_In)24* MOD_G* MOD_1Analog Modulation In, all channelsA_In22nc* MOD_3NCA_In21

* MOD-n input = 0 - 5.0V



J7 Control 2

26 way Amplimite High Density IDC D-type

<u>Pin</u>	<u>Main</u>	<u>(Alt)</u>	Description	Type	<u>Pin</u>	
13	EQ_EN		External Equip Enable	C_Out	26	C_Out
12	/RST		- Reset	D_ln	25	DGnd
11	DAC_O		0-10V Analog output	A_Out	24	DGnd
10	ADC_1		0-10V ADC input	A_In	23	DGnd
9	dnc	(ADC_2)	DO NOT CONNECT	A_In	22	DGnd
8	DIO0	(MA0)	Async digital I/O bit0	D_ln	21	DGnd
7	DIO1	(MA1)	Async digital I/O bit1	D_ln	20	DGnd
6	DIO2	(MA2)	Async digital I/O bit2	D_ln	19	DGnd
5	DIO3		Async digital I/O bit3	D_I/O	18	DGnd
4	DIO4		Async digital I/O bit4	D_I/O	17	DGnd
3	DIO5		Async digital I/O bit5	D_I/O	16	DGnd
2	DIO6		Async digital I/O bit6	D_I/O	15	DGnd
1	DIO7		Async digital I/O bit7	D_I/O	14	DGnd

J5 AO Interlock

4 way Binder 719

<u>Pin</u>		Description	Туре
1	AO_INT+	Interlock/Thermostat	A_Out
2	AO_INT-	Interlock/Thermostat	A_In
3	VB1	Sensor Bias	A_Out
4	Temp	Sensor Signal	A_In

J5 Connections



Note: Some versions of the iHSA may be fitted with 3-pin connector for J5 In this case, INTL+ and INTL- are on pins 1 and 2 respectively.



15.1 Example external connections

J6 Connection for Image mode with:

External Trigger, Clock inputs External amplitude control MOD_G

Synchronous data output signal (x1) Synchronous analog out[t signal (x1)



J7 Connection for:

Analog ADC read Analog output write



J7 Connection for:

Reset switch

Equipment relay control





16 Profile Pin control input characteristics

For the Sweep and Multi–level modulation modes, the output responds to a change initiated by the profile control inputs within 100nsec.

The Profile inputs are multifunctional and depend on the mode of operation.

- P0 corresponds to Ch0 (iHSA output J1) P1 corresponds to Ch1 (iHSA output J2)
- P2 corresponds to Ch2 (iHSA output J3)
- P3 corresponds to Ch3 (iHSA output J4)

Connections on J6 for external Profile control of RAMP or Multi-level modulation.







3.3mm dia (x4)



TE "Amplimite",050 IDC High Density "D" with latch

Mounting Holes

4 x 3,3mm diameter

Figure 1: Driver Installation, iHSA-4





Figure 2: Driver Block Diagram, iHHS-4



The input Bragg angle relative the optic face normal is:

$$\theta_{\text{Bragg}} = \frac{\lambda.\text{fc}}{2.\text{v}}$$

The separation angle between the Zeroth order and the First order is:

$$\theta_{\text{SEP}} = \frac{\lambda.\text{fc}}{v}$$

The scan angle of the First order is:

$$scan = \frac{\lambda \cdot \Delta f}{v}$$

Optical rise time for a Gaussian input beam is approximately:

θ

$$t_r = \frac{0.65.d}{v}$$

where:

 $\begin{array}{l} \lambda = \text{wavelength} \\ \text{fc} = \text{centre frequency} \\ \Delta \text{f} = \text{frequency sweep bandwidth} \\ \text{v} = \text{acoustic velocity of AO interaction material} \\ = 4.21 \text{mm/usec (TeO_2)} \\ = 3.63 \text{mm/usec (PbMoO_4)} \\ = 5.7 \text{mm/usec (Quartz)} \end{array}$

 $d = 1/e^2$ beam diameter

Figure 3: Typical AOD Set-up



17 Appendices

17.1 Expansion PCB for J6, J7





17.2 Image File format

Disclaimer: This document describes the current design philosophy. Details may change.

To simplify image file generation, a Windows software program *iHHS Image File Generator* is available as a download from <u>www.isomet.com /software.html</u>.

To view and edit Image files, we recommend downloading a hex editor software program such as Hex Editor Neo by HDD Software Ltd.

A full description of the file format is given in the document *Image Data Format* also available as a download from <u>www.isomet.com /manual.html</u>